REMARKS

New claims 33-35, which depend from claim 1, have been added.

New independent claim 36, along with dependent claims 37-38, has been added.

Claims 1-23 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman in view of Barnes. Applicant respectfully traverses the rejections and requests reconsideration.

Claim 1 recites "storage means for holding packets of the input packet streams at addressable locations each identifiable by an address." The Examiner continues to point to Chapman's input buffers as described at col. 2, lines 4-5. The buffers taught by Chapman perform traffic buffering. With reference to Figure 3, Chapman teaches input buffer 320/324. The input buffer 320/324 is a FIFO queue for temporary packet storage (see, col. 7, line 51).

Applicant has previously pointed out that there is no teaching or suggestion in Chapman for these buffers 320/324 being addressable. The Examiner's response to this argument is that the Chapman input buffers 320/324 are interpreted as either being identified as (1) physical memory addresses or 2) pointers to the packet's location in memory. Applicant strongly disagrees with the Examiner's interpretation and application of the Chapman prior art.

First, it is improper for the Examiner to make more of the prior art teachings than is actually present. Chapman clearly teaches that the input buffers 320/324 are FIFO queues. Chapman does not specify that these FIFO queues are in any way addressable. The operation of a FIFO queue is well understood: only the "first-in" data item in the queue can be read out of the queue. Given this functional operation of the FIFO queue, the data storage locations within the queue ARE NOT AND NEED NOT be individually addressable. Why would one specify the use of a FIFO queue, where the functional operation is to store data in the order received and release that data in the order received, and then make individual data locations in the queue addressable? Addressing of the locations in the FIFO queue is not necessary, because the location of the data to be output from the queue is known and accessible without providing an addressing scheme (that data is always at the end of the queue ready to be pushed out). Further, the data which is buried in the middle of the queue does not need to be addressed and retrieved because that would destroy the functional operation of a FIFO architecture which controls the way data is output such that the output data is always that data which was first input.

Second, there is no suggestion in Chapman that the input buffers 320/324 have "(1) physical memory addresses." Chapman does not mention any form of addressing associated with the buffers 320/324, and further those skilled in the art would recognize that addressing, or

assigning addresses to the data storage locations inside a FIFO buffer, is unnecessary and contrary to their standard mode of operation.

Third, there is no suggestion in Chapman that the data stored in the FIFO queues of Chapman constitutes "2) pointers to the packet's location in memory." This appears to be a form of indirect addressing argument. The Examiner appears to argue that the FIFO buffers are not addressed, but instead the data stored therein is an address or pointer to a memory location. Again, Chapman does not mention any form of addressing, either direct or indirect, associated with the buffers 320/324. The data stored by Chapman in the FIFO queue packet data, not any sort of address or pointer data.

The Examiner additionally cites to Barnes with respect to the Chapman buffers and suggests that Barnes' memory management scheme could be used to replace the Chapman buffers. What would be the motivation for such a modification? The Chapman system operates correctly and as described with FIFO queuing of incoming data. There is no indication that performance of the Chapman system is adversely affected by having access only to the data which was first put into the FIFO queue. There is no indication that performance of Chapman's system would improve if the system could instead address and access data which is buried in the middle of the queue. In fact the whole point of Chapman's operation is to process the data in the order in which it is received. This is supported through the data buffering functionality of a FIFO-type queue. Chapman col. 7, lines 50-59 clearly teaches that the queues are designed as a "temporary storage mechanism" holding the data until a routing decision can be made. Still further, there is no functionality identified by the Examiner in Chapman which could control and handle addressed data in the input buffer in any manner other than FIFO. It connect be said that substitution of Barnes' scheme for the Chapman FIFO buffers is a simple operation, and it is not clear how Chapman's process would benefit from the substitution such that it would obvious for one skilled in the art to try.

In view of the foregoing, Applicant submits that the Examiner has failed to prove the prima facie case. The Chapman reference does not teach addressable memory for the FIFO queues. The Chapman reference does not need or suggest the ability to individually address buried locations in the buffer queues. There is no indication as to how the Barnes memory management scheme could be integrated and used in the Chapman process, and further there is no suggestion that the Barnes memory management scheme should or could replace the FIFO buffers of Chapman.

Claim 1 further recites "***a packet allocation data structure holding*** for each new incoming packet a source identifier identifying the origin of the packet and ***the address in the storage means where the packet is held***" (emphasis added). This limitation links to the previously discussed "***storage means for holding*** packets of the input packet streams ***at addressable locations*** each identifiable by an address." Since Chapman does not teach or suggest the FIFO queue having addressable locations "for holding packets of the input packet streams," it is clear that Chapman does not teach or suggest "a packet allocation data structure" which holds the addresses of the packets in the storage means.

The Examiner points to Chapman's routing table as described at col. 7, lines 65-67 and col. 10, lines 5-12. Applicant argued that the routing table maps the destination address of an incoming data packet to a switch output port (col. 7, lines 65-67). In other words, the routing table contains information of the form –any packet having a destination address of A should be routed to output port B. Chapman does not teach having the routing table include information specifying the origin of an individual packet, AND (with reference to the recited claim language) Chapman does not teach having the routing table store "the address in the storage means where the packet is held". One reason for this is that Chapman's FIFO is not addressable. Another reason for this is that Chapman is concerned only with the first-out data whose location in the system is well known (it is at the output of the FIFO queue) and thus does not need to be specifically addressed. Still another reason for this is that Chapman does not need to have access to data buried in the middle of the FIFO queue at any time before that data becomes available in normal course at the output of the queue.

In response, the Examiner argues that well known memory mapping schemes implicate "the location/address (within buffer/queue) of the incoming packet." Office Action, page 3. In other words, it is well known, in the context of a routing table, to store "a source identifier identifying the origin of the packet and the address in the storage means where the packet is held" as claimed. Notably, the Office Action fails to cite to any prior art documentation which supports the Examiner's position. In view of the absence of any specifically identified prior art, Applicant respectfully disputes the Examiner's position and requests that the Examiner prove the prima facie case by citation to supporting prior art. If the use of a packet allocation data structure as recited in claim 1 is inherent, or otherwise well known to those skilled in the art, then the Examiner should be able to cite to prior art showing a routing table, like that taught by Chapman, which includes data on packet origin AS WELL AS the address where that packet to

be routed is stored in a buffer memory. Applicant does not believe that such art exists. The only teaching for the claimed packet allocation data structure comes from Applicant's own disclosure. Absent citation to supporting prior art, the Examiner cannot reasonably assert that the claimed packet allocation data structure is known or obvious.

Furthermore, even if known memory-mapping schemes were to use packet source identifiers and addressable buffer storage addresses, such schemes would still not teach or suggest holding this information for each packet in a "data structure" as claimed. The prior art may hold the information as distributed information, but there is no indication for storage of the information together in a data structure. The provision of a data structure with the claimed information allows an algorithm or process which uses the information to be implemented more efficiently. Better control over removal of data packets from the addressable storage buffer is possible, and this can ensure that bandwidth is maximized and that packets are handled in the correct order.

Claim 1 still further recites "the packet allocation data structure further holding information identifying the ***output ports*** associated with the intended ***destinations*** of a held packet." Again, we are discussing the packet allocation data structure. The Examiner points to the routing table. While Chapman's routing table identifies an output port, the claim recites the identification of output ports (plural) for each held packet, those output ports being for intended destinations (again plural). There is no teaching or suggestion in Chapman for this aspect of the claimed invention.

In view of the foregoing, Applicant respectfully submits that claim 1 is patentable over the cited prior art.

Claim 8 includes similar limitations as claim 1, and thus Applicant submits that claim 8 is patentable over the cited prior art for at least the same reasons as claim 1.

Claim 11 is a method claim with similar limitations as claim 1, and thus Applicant submits that claim 11 is patentable over the cited prior art for at least the same reasons as claim 1.

Claim 15 recites "a packet allocation table for associating a source and at least one destination for a particular packet with the address location in the addressable memory where the particular packet is stored." This limitation is similar to the "packet allocation data structure" recited in claim 1. Applicant submits that claim 15 is patentable over the prior art for at least the reasons recited above with respect to the "packet allocation data structure" of claim 1. Claim 15

further recites "an addressable memory which stores receives packets at a plurality of address locations in the memory." This limitation is similar to the "storage means" limitation of claim 1. Applicant submits that claim 15 is patentable over the prior art for at least the reasons recited above with respect to the "storage means" of claim 1.

Claim 18 is a method claim with similar limitations as claim 15, and thus Applicant submits that claim 18 is patentable over the cited prior art for at least the same reasons as claim 15.

Claims 24-31 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chapman in view of Barnes and Wegner. Claims 24-31 have been canceled.

New claim 36 has been added and is believed to be patentable over the prior art. The cited prior art references fail to teach or suggest the addressable memory, source-to-destination matrix, destination pointers and processor (with implemented operations) as claimed.

Applicant respectfully submits that all claims of the application are in condition for favorable action and allowance.

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